



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : **MAIL STOP: AF**  
Tomoji HAMADA : **Confirmation No. 4745**  
Serial No. 10/623,655 : **Docket No. 2003\_0996A**  
Filed July 22, 2003 : **Group Art Unit 2811**  
SEMICONDUCTOR APPARATUS : **Examiner J. M. Im**

---

**THIRD REQUEST FOR RECONSIDERATION**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Responsive to the Final Office Action mailed March 25, 2005, and the telephonic interview conducted with Examiner Im on December 30, 2005, the time for responding thereto being extended for (2) months in accordance with a Petition for Extension of Time submitted herewith, please consider the following remarks.

Initially, the courtesies extended by Examiner Im in conducting the telephonic interview on December 30, 2005, are greatly appreciated. During this interview, the following limitation of claim 1 was discussed,

**wherein said semiconductor device is connected with said  
external electrodes via said first through-hole wiring  
and said internal wiring.**

Specifically, Applicant's undersigned representative pointed out to Examiner Im that in order for this limitation to be read on Hung et al., assuming arguendo that conductive layer 216 is properly construed as ground electrodes, microstrip 112 must be connected with the first through-hole wiring 126 and the internal wiring 218. It was then explained why microstrip 112 is not connected with neither wiring 126 nor wiring 218, whereby semiconductor device 110 is not

connected to ground electrodes or conductive layer 216 via the first through-hole wiring 126 and the internal wiring 218.

Specifically, Examiner Im's attention was directed to the initial paragraph in column 4 of Hung et al., which states that land region 106, within which is located microstrip 112, is "devoid of any conductive coating", and therefore, the microstrip cannot be connected with conductive layer 216 via the first through-hole wiring 126 and the internal wiring 218.

Examiner Im was in apparent agreement, and stated that were a response filed the current rejections of record would not be maintained if upon further consideration it is determined that the aforementioned limitation does indeed define around Hung et al.

Because in Hung et al., the microstrip 112 is not connected with neither wiring 126 nor wiring 218, the semiconductor device 110 is not connected to conductive layer 216 via wiring 126 and wiring 218. Thus, claim 1 is not anticipated by Hung et al. Karnezos does not resolve this deficiency of Hung et al., and accordingly, claim 1 is also not obvious over a combination of Hung et al. and Karnezos, whereby claims 1-19 are allowable.

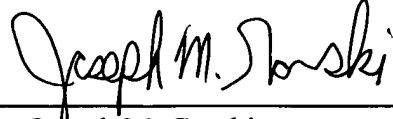
Also during this interview, Examiner Im indicated that Fig. 1 is inaccurate in that this figure apparently shows dielectric layers 13a and 13b to not be coextensive, whereas the remaining figures do show such a coextensive relationship. Accordingly, a replacement formal drawing for Figure 1 is provided herewith, which shows dielectric layers 13a and 13b to be coextensive.

In view of the above, it is respectfully submitted that the application is in condition for allowance, and an early Notice of Allowance is earnestly solicited.

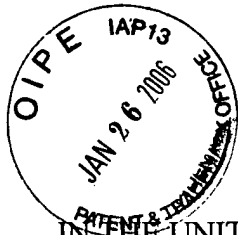
If after reviewing these remarks, the Examiner believes that any issues remain which must be resolved before the application can be passed to issue, the Examiner is invited to contact the Applicant's undersigned representative by telephone to resolve such issues.

Respectfully submitted,

Tomoji HAMADA

By:   
\_\_\_\_\_  
Joseph M. Gorski  
Registration No. 46,500  
Attorney for Applicant

JMG/nka  
Washington, D.C. 20006-1021  
Telephone (202) 721-8200  
Facsimile (202) 721-8250  
January 26, 2006



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : Attorney Docket No. 2003\_0996A  
Tomoji HAMADA : **Confirmation No. 4745**  
Serial No. 10/623,655 : [Group Art Unit 2811  
Filed July 22, 2003 : Examiner Junghwa M. IM]  
SEMICONDUCTOR APPARATUS : **Mail Stop AF**

---

**SUBMISSION OF REPLACEMENT FORMAL DRAWING**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Submitted herewith is a replacement formal drawing for Fig. 1 (1 sheet, A4 paper).

Respectfully submitted,

Tomoji HAMADA

By:

Joseph M. Gorski  
Registration No. 46,500  
Attorney for Applicant

JMG/nka  
Washington, D.C. 20006-1021  
Telephone: (202) 721-8200  
Facsimile: (202) 721-8250  
January 26, 2006